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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|-----------------|-------------|----------------------|---------------------|------------------|
| 10/677,560 | 10/01/2003 | Michael Lee Workman | Pillar 716 | 3994 |
| 7590 | 09/17/2004 | | | |
| EXAMINER | | | | |
| PARK, ILWOO | | | | |
| ART UNIT | | PAPER NUMBER | | |
| 2182 | | | | |

DATE MAILED: 09/17/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/677,560

Applicant(s)

WORKMAN ET AL.

Examiner

Ilwoo Park

Art Unit

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 01 October 2003.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-23 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-23 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date <u>2/6/04, 05/3/04</u> | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

1. Claims 1-23 are presented for examination.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

3. Claims 1, 2, 14, 17, and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over El-Batal et al., US patent application publication No. US 2003/0221061 A1 and Okada, US patent No. 6,381,675.

As to claim 1, El-Batal et al teach a coupling circuit for an ATA storage device, comprising:

a first Serial ATA controller-side transceiver [e.g., fig. 6 and physical layer interface 760] receiving a first Serial ATA communication path;

a second Serial ATA controller-side transceiver [e.g., physical layer interface 761] receiving a second Serial ATA communication path;

a Serial ATA device-side transceiver [e.g., physical layer interface 912 in order to transmit and receive serialized datastream to and from the physical layer interfaces at the controllers side; disks are Serial ATA disks which are inputting and outputting serialized datastream in accordance with a Serial ATA Specification in paragraph 0051];

coupling circuit switches [e.g., switches 741] which selectively coupling either the first Serial ATA controller-side transceiver or the second Serial ATA controller-side

transceiver to the Serial ATA device-side transceiver based on the logic state of a path control line.

Though El-Batal et al disclose the coupling circuit switches each associated with each of ATA disks for selectively connecting an ATA communication path of each ATA disk with an ATA path of one of multiple controllers [fig. 7A; paragraph 0057], El-Batal et al does not expressly disclose a microcontroller adapted to control the coupling circuit switches for the ATA connection. Okada teaches coupling circuit switches [figs 1-3] each associated with each of ATA disks for selectively connecting an ATA communication path of each ATA disk with an ATA path of one of multiple controllers and a microcontroller [col. 5, lines 47-50] adapted to control the coupling circuit switches for the ATA connection. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of El-Batal et al and Okada because they both teach coupling circuit switches each associated with each of ATA disks for selectively connecting an ATA communication path of each ATA disk with an ATA path of one of multiple controllers and the Okada's teaching of a microcontroller adapted to control the coupling circuit switches for the ATA connection would increase user friendliness of ATA communication path control [El-Batal et al: paragraph 0005].

4. As to claim 2, El-Batal et al teach an out of band squelch control component [Serial ATA specification: paragraph 0005] for activating the first Serial ATA controller-side transceiver, the second Serial ATA controller-side transceiver, and the Serial ATA device-side transceiver.

5. As to claim 14, Okada teaches [col. 6, lines 13-24] a data storage system for assigning control of ATA storage devices, wherein each ATA storage device connects

through coupling circuit switches to storage controllers, comprising:

- a host sending an I/O command; and

- a first storage controller receiving the I/O command and commanding the coupling circuit switches to connect the ATA storage devices identified in the I/O command to the first storage controller.

However, Okada does not explicitly disclose the ATA storage devices are serial ATA storage devices. El-Batal et al teach each of serial ATA storage devices connected through coupling circuit switches to storage controllers. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to include the El-Batal et al's teaching of ATA storage devices being serial ATA storage devices in order to simplify switching circuitry of Okada or increase adaptability of the prevailing serial ATA storage devices [El-Batal et al: paragraph 0049].

6. As to claim 17, Okada teaches [col. 6, lines 13-24] a data storage subsystem for controlling ATA storage devices, wherein each ATA storage device connects through coupling switches to storage controllers, comprising:

- a first storage controller; and

- a second storage controller, wherein the first storage controller assigns the ATA storage devices to the first storage controller or the second storage controller and commands the coupling circuit switches to correspondingly connect the ATA storage devices to the first storage controller or the second storage controller.

However, Okada does not explicitly disclose the ATA storage devices are serial ATA storage devices. El-Batal et al teach each of serial ATA storage devices connected through coupling circuit switches to storage controllers. Therefore, it would have been

obvious to one of ordinary skill in the art at the time the invention was made to include the El-Batal et al's teaching of ATA storage devices being serial ATA storage devices in order to simplify switching circuitry of Okada or increase adaptability of the prevailing serial ATA storage devices [El-Batal et al: paragraph 0049].

7. As to claim 23, Okada teaches [fig. 1] a coupling circuit for an ATA storage device, comprising:

means for receiving a first ATA communication path;

means for receiving a second ATA communication path;

means for coupling either the first ATA communication path or the second ATA communication path to the ATA storage device; and

a microcontroller [col. 5, lines 47-50] adapted to control the coupling circuit switches.

However, Okada does not explicitly disclose the ATA storage device being a serial ATA storage device. El-Batal et al teach an ATA storage device being a serial ATA storage device selectively coupled to either a first ATA communication path or a second ATA communication path. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to include the El-Batal et al's teaching of a serial ATA storage device in order to simplify switching circuitry of Okada or increase adaptability of the prevailing the serial ATA storage device.

8. Claims 8-11 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Pinson, US patent No. 6,256,748 in view of El-Batal et al., US patent application publication No. US 2003/0221061 A1.

As to claim 8, Pinson teaches a method of controlling storage devices in a data

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storage subsystem, comprising:

connecting the storage devices to a first storage controller [col. 4, lines 20-21];

reading the identity of each of the storage devices;

dividing the storage devices into set(s) [col. 5, lines 45-49];

assigning each set to the first storage controller or a second storage controller [col. 5, lines 45-49]; and

coupling the storage devices as assigned to the first storage controller or the second storage controller [col. 5, lines 45-49].

However, Pinson does not teach the storage devices are serial ATA storage devices; actually, Pinson teaches two controllers each controller for taking over the control of the SCSI storage devices connected to other controller in case of a failure of the other controller [col. 4, lines 39-56; fig. 4]. El-Batal et al teach two controllers each controller for taking over [paragraph 0047] the control of Serial ATA storage devices connected to other controller in case of a failure of the other controller instead of expensive SCSI storage devices. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to include the El-Batal et al's teaching of Serial ATA storage devices instead of SCSI storage devices in order to reduce cost to or increase simplicity for manufacture [El-Batal et al: paragraph 0049].

9. As to claim 9, Pinson teaches receiving a host I/O command in the first storage controller [col. 7, lines 40-45].

10. As to claim 10, Pinson teaches first controller instructing the second storage controller to couple the set(s) of storage devices [paragraph 0048].

11. As to claim 11, Pinson teaches coupling the set(s) of storage devices to the first storage controller first controller and notifying the second storage controller [col. 5, lines 31-38].

12. As to claim 13, Pinson teaches coupling all the storage devices to the first storage controller and coupling all the storage devices to the second storage controller if the first storage controller fails [col. 7, lines 60-64].

13. Claim 21 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Okada, US patent No. 6,381,675, El-Batal et al., US patent application publication No. US 2003/0221061 A1, and Cargemel et al., US patent No. 6,295,609.

As to claim 21, Okada teaches a method of restoring operation of an ATA storage device, comprising:

detecting the ATA storage device has failed to respond to an I/O command within a predetermined time [col. 6, lines 33-41].

However, Okada does not disclose commanding a coupling circuit to power down the ATA storage device for a predetermined time; and commanding a coupling circuit to power up the ATA storage device. Cargemel et al teach a method of restoring operation of a storage device comprising: commanding a coupling circuit [interconnect card CC] to power down [col. 6, lines 66-67] the storage device failed for a predetermined time; and commanding a coupling circuit to power up [col. 7, lines 1-3] the storage device. Okada and Cargemel et al do not explicitly disclose the ATA storage devices being serial ATA storage devices; El-Batal et al teach restoring operation of serial ATA storage devices. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Okada, Cargemel et al, and El-Batal et

al because they both teach restoring operation of a storage device, connected two storage controllers through a coupling circuit, comprising detecting a failed storage device and Cargemel et al's teaching of commanding a coupling circuit to power down the storage device failed for a predetermined time and commanding a coupling circuit to power up the storage device automatically would increase user friendliness of repairing the failed storage device [col. 7, lines 43-45 of Cargemel et al] and the El-Batal et al's teaching of ATA storage devices being serial ATA storage devices would increase simplify switching circuitry of Okada or increase adaptability of the prevailing serial ATA storage devices.

14. As to claim 22, Okada teaches [fig. 1] a coupling circuit for a storage device, comprising:

- receiving a first communication path at a first controller-side;
- receiving a second communication path at a second controller-side;
- a storage device-side;
- coupling circuit switches selectively coupling either the first controller-side or the second controller-side to the storage device-side; and
- a microcontroller [col. 5, lines 47-50] adapted to control the coupling circuit switches.

However, Okada does not disclose transceivers at the first controller-side for the first communication path, at the second controller-side for the second communication path, and at the storage device-side. And Okada does not disclose the microcontroller also controlling the power to the storage device. El-Batal et al teach each transceiver at a first controller-side, a second controller-side, and a storage device-side. And Cargemel et

al teach a microcontroller controlling the power to the storage device [fig. 2; col. 6, line 55-col. 7, line 10]. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to include transceivers at the first controller-side for the first communication path, at the second controller-side for the second communication path, and at the storage device-side in order to increase path signals integrity or reliability and to implement into the microcontroller of Okada the Cargemel et al's teaching of a microcontroller controlling the power to the storage device in order to increase user friendliness of repairing the failed storage device.

15. Claims 3-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over El-Batal et al and Okada as applied to claim 1 above, and further in view of Cargemel et al., US patent No. 6,295,609.

As to claim 3, El-Batal et al and Okada do not disclose the microcontroller includes a processor coupled to a power switch and coupled to the coupling circuit switches. Cargemel et al teach a microcontroller controlling the power to the storage device [fig. 2; col. 6, line 55-col. 7, line 10]. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to implement the Cargemel et al's teaching of a microcontroller controlling the power to the storage device into the microcontroller of El-Batal et al and Okada in order to increase user friendliness of repairing the failed storage device.

16. As to claim 4, El-Batal et al and Okada teach the microcontroller includes a processor coupled to a set of logics [Okada: col. 4, lines 50-55] controlled by a pulse input. However, El-Batal et al and Okada do not disclose the set of logics includes D flip-flops that are coupled to a power switch and coupled to the coupling circuit switches.

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Cargemel et al teach the microcontroller coupled to a power switch and coupled to a coupling circuit switches. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to implement the Cargemel et al's teaching of a microcontroller controlling the power to the storage device into the microcontroller of El-Batal et al and Okada in order to increase user friendliness of repairing the failed storage device. Further, Cargemel et al do not disclose the set of logics including a set of D flip-flops. It is well known in the art that the set of logics controlled by a pulse input to latch the pulse input signal includes a set of D flip-flops for simplicity.

17. As to claim 5, El-Batal et al and Okada teach the microcontroller is programmed to as follows switch the coupling circuit to a first storage controller; and switch the coupling circuit to a second storage controller. However, El-Batal et al and Okada do not disclose power up the storage device; and power down the storage device. Cargemel et al teach [col. 5, lines 3-19; col. 6, line 55-col. 7, line 11] the microcontroller is programmed to as follows: switch the coupling circuit to a first storage controller; switch the coupling circuit to a second storage controller; power up the storage device; and power down the storage device. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to implement the Cargemel et al's teaching of a microcontroller controlling power up/down the storage device into the microcontroller of El-Batal et al and Okada in order to increase user friendliness of repairing the failed storage device.

18. As to claim 6, Cargemel et al teach [col. 6, line 55-col. 7, line 11] the microcontroller further programmed to as follows: write data to a memory; read data from the memory; and read the status of the coupling circuit.

19. As to claim 7, Cargemel et al teach [col. 4, lines 7-13; col. 5, lines 3-19; col. 6, line

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55-col. 7, line 11] the status includes information on whether the storage is coupled to the first controller-side or the second controller-side, the storage is powered up or down, the communication status, and/or the board revision and code revision levels of the coupling circuit.

20. Claims 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Pinson and El-Batal et al as applied to claim 8 above, and further in view of Walker, US patent No. 5,848,230.

As to claim 12, Pinson and El-Batal et al teach dividing the storage devices in two sets; however, they do not disclose a spare. Walker teach dividing the storage devices in two sets plus a spare [col. 6, lines 8-17]. Therefore, it would have been obvious to one of ordinary skill in the art to include the Walker's teaching of spare disk in order to further increase reliability/conveniency of the storage subsystem.

21. Claims 15, 16, and 18-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Okada and El-Batal et al as applied to claim 8 above, and further in view of Pinson, US patent No. 6,256,748.

As to claims 15 and 18, Okada and El-Batal et al do not expressly disclose the first storage controller is programmed to read the identity of each of the Serial ATA storage devices and divide the Serial ATA storage devices into set(s).

As to claim 16, Okada and El-Batal et al do not expressly disclose the first storage controller is programmed to read the identity of each of the Serial ATA storage devices and divide the Serial ATA storage devices into set(s).

Pinson teaches [col. 5, lines 39-49] the first storage controller or the second storage controller is programmed to read the identity of each of the Serial ATA storage

devices and divide the Serial ATA storage devices into set(s). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to include the Pinson's teaching of the first storage controller or the second storage controller programmed to read the identity of each of the Serial ATA storage devices and divide the Serial ATA storage devices into set(s) would increase flexibility in configuration of active operation and failover operation of Okada and El-Batal et al.

22. As to claim 19, Okada teaches the first storage controller assigns the set(s) to the second storage controller and instructs the second storage controller to switch to the set(s) of Serial ATA storage devices [fig. 7; col. 5, line 65-col. 7, line 10].

23. As to claim 20, Okada teaches the first storage controller assigns the set(s) to the second storage controller, switches the set(s) to the second storage controller, and notifies the second storage controller of the assignment [fig. 7; col. 5, line 65-col. 7, line 10].

Conclusion

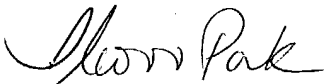
24. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ilwoo Park whose telephone number is (703) 308-7811 (will be changed to (571) 272-4155 during mid October, 2004). The examiner can normally be reached on Monday through Friday from 9:00 AM to 5:30 PM. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jeffrey A Gaffin can be reached on (703) 308-3301 (also will be changed to (571) 272-4146 during mid October, 2004). The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306. Any inquiry of a general nature or relating to

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the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

ILWOO PARK
PRIMARY EXAMINER



Ilwoo Park

Primary Examiner

September 14, 2004